

1 (C) AMENDMENTS TO THE CLAIMS

2 1. (Currently Amended) A semiconductor MOSFET structure having improved  
3 electrostatic discharge tolerance, the structure comprising:  
4 a semiconductor substrate having an active device surface;  
5 in said surface, a MOSFET source region and a MOSFET drain region separated  
6 by a channel region;  
7 a P-type dopant region subjacent said drain region and having a dopant  
8 concentration and predetermined dimensions ~~[[ such ]]~~ selected for increasing inherent  
9 parasitic transistor gain of said MOSFET structure ~~[[ is-increased ]]~~ for improving said  
10 electrostatic discharge tolerance.

11 2. (Original) The structure as set forth in claim 1 comprising:  
12 said MOSFET is a N-channel MOSFET wherein said P-type dopant region has  
13 said dopant concentration and said predetermined dimensions set for increasing drain-  
14 to-substrate capacitance thereby.

15 3. (Original) The structure as set forth in claim 1 comprising:  
16 said MOSFET is a N-channel MOSFET wherein said P-type dopant region has  
17 said dopant concentration and said predetermined dimensions set such that the  
18 MOSFET trigger voltage is decreased thereby.

19 4. (Original) The structure as set forth claim 1 wherein breakdown voltage of said  
20 parasitic transistor is tailored by depth of the P-type dopant region with respect to said  
21 surface and said substrate.

22 5. (Currently Amended) The structure as set forth in claim 1 wherein said MOSFET  
23 is a N-channel MOSFET located in a P-type dopant well in said epitaxial layer and  
24 surface concentration of the dopant ions in the P-deep region is approximately an order

1 of magnitude greater than that of the dopant ions at the P-well [[ 209 ]] surface  
2 concentration.

3 6. (Currently Amended) The structure as set forth in claim 3 comprising:  
4 a pair of MOSFETs, including a paired N-MOSFET, and a paired P-MOSFET,  
5 wherein said paired N-MOSFET and said paired P-MOSFET are connected in a push-  
6 pull configuration.

7 7. (Original) The structure as set forth in claim 6 wherein the P-deep implant region  
8 in both the P-MOSFET and the N-MOSFET reduces effective base width of parasitic  
9 transistors therein via reduction of substrate-to-drain spacing.